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Anyway back to the topic. It is not as if people are getting hammered about some of this new tooling. We have all known for years that the commercial semiconductors are really really good at verifying what is going on at the gate level, but really poor at everything else. Now they are getting better at verifying the bit level. Its a strategic play and is the first cog in the wheel to the neutrons CRACK Vehicle Tracking 2017 X64 (64bit) Product Key I agree, I wish they had said. But I also agree with the industry complaints that it wasnt comprehensive enough. That I agree with also. But I also think that it is a direct attack on the underlying problem. Bit Level Verification, redundancy and robustness are bigger problems than device level verification, I think. We are not aware of any new attacks on bit-level verification. There is alot of study going on in that area. So theres 1 big problem 1 small one. If bit-level verification is the keystone then perhaps bit-level verification is the keystone. If one can do that then that is a good start. So you need to make sure that the device doesnt leak information. Which is where the security chip comes into play. By performing root of trust on the data and doing signal analysis in real-time. So we can drive a proximity warning in the vehicle. If its too hot we put a braking system on the vehicle. If its too cold we put on a heating system etc. We use a conventional wireless radio link to send the data stream. Even if the device is compromised this cant happen because at all stages it is a multiple endpoint cryptographic handshake (for example if a virus infected the device its not sending that information as soon as it enters our system so when the drive gets back to you it sends the data as clean as it came out.

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While that's interesting and all, I still think the coolest thing I've seen is the Archipelago FPGA. They are still working to add things like MAC to transform it into a real contender. However, making that thing work with or without MAC on a good toolchain (esp Qflow w/ YoSys ) at 45nm or even 90nm would be the best thing a person could do for OSS hardware. Combined with breadboards or existing maker products, it would make hardware design a lot more plug-and-play with us able to understand everything down to the logic slices. And for pros, down to the transistors as the FPGA itself and tooling are open to verification. People could even respin it on new fabs if they wanted. I mean, the difference between requiring two doses versus three may be life or significant, perhaps-practically-impossible-to-detect harm to the individual, but to an MBA acolyte that's merely a 50% more sales no-brainer worthy of investing in investing in goal-seeking researchers. (And, just because vaccines aren't nearly as big a seller as anti-depressants or pain meds, that doesn't mean their profits aren't literally hundreds and hundreds of millions of dollars, which they are.) The last thing vax tech needs are the people who decide that ten people dying because the seat belt buckle has issues are not enough to recall the vehicles. One reason I found it so interesting was that it wasn't an important product but it was a major win. The company was in the sector of radar/radar like detectors that directly measured the signals from radars, by using that knowledge they could tell where a military radar was and provide threat assessment. The company did all the calculations themselves so they had some pretty nerdy people in the back end doing the stuff for them. A problem developed in

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some of their software where they would set the system to alert when a radar or radars were detected, and set it to an alert level of where they thought the radar was. 5ec8ef588b

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